IN THE CLAIMS

1. (currently amended) A method of fabricating a microelectronic assembly comprising the steps of:

(a) providing an active microelectronic element including active devices in an active element body and active element contacts exposed at a surface of said active element body and electrically connected to said active devices;

(b) separately providing an interconnect element including an interconnect element body, ~~and~~ interconnect conductors having electrical conductivity at least equal to that of copper in ~~an~~ said interconnect body, and contact pads electrically connected to said interconnect conductors ;

(c) joining said interconnect element to said active element so as to connect said interconnect conductors to said active devices, said joining step including forming substantially rigid metal-to-metal interconnects between said active element contacts and said contact pads using a substantially solid-phase bonding process; and

(d) connecting terminals to at least some of said interconnect conductors so that said terminals are movable with respect to said interconnect body and so that said terminals are exposed for connection to an external substrate.

2. (original) A method as claimed in claim 1 wherein said interconnect element body with said conductors has a coefficient of thermal expansion substantially equal to the coefficient of thermal expansion of said active element body

3. (original) A method as claimed in claim 1 wherein said step of connecting terminals is performed after said step of joining said interconnect element to said active element.

4. (original) A method as claimed in claim 1 wherein said step of connecting terminals is performed before said step of joining said interconnect element to said active element.

5. (original) A method as claimed in claim 1 wherein at least some of said interconnect conductors include a metal selected from the group consisting of copper and copper alloys.

6. (original) A method as claimed in claim 1 wherein said active element includes a plurality of active devices in plural regions of said active element body, the method further comprising the step of severing said regions of said active element body from one another and severing portions of said interconnect body from one another after joining the interconnect body and active body so as to form individual assemblies, each including one or more semiconductor chips and a portion of the interconnect body joined to such one or more chips.

7. (original) A method as claimed in claim 6 wherein said step of connecting terminals is performed before said severing step so that each of said individual assemblies resulting from said severing step includes a plurality of said terminals.

8. (cancel)

9. (cancel)

10. (cancel)

11. (currently amended) A method as claimed in claim ~~10~~ 1 wherein said ~~bonding step~~ substantially solid-phase bonding process includes bonding masses of bonding metal consisting predominantly of gold between said active element and bonding pads on said interconnect element.

12. (currently amended) A method as claimed in claim ~~8~~ 1 wherein said bonding step includes forming said metal-to-metal interconnects by eutectic bonding or diffusion bonding.

13. (currently amended) A method as claimed in claim ~~8~~ 1 wherein said joining step includes sealing said interconnect body to said active microelectronic element.

14. (original) A method as claimed in claim 13 wherein said sealing step is performed simultaneously with said bonding step.

15. (original) A method as claimed in claim 1 wherein said step of providing terminals includes connecting said terminals to said at least some of said interconnect conductors through leads and then deforming said leads by displacing said terminals away from said interconnect body so as to bend said leads.

16. (original) A method as claimed in claim 15 wherein said step of connecting said terminals includes providing said terminals on a dielectric interposer.

17. (currently amended) A method of joining microelectronic elements comprising the steps of:

(a) juxtaposing

(1) a first microelectronic element having a first body with a body surface and metallic contact bumps projecting from said body surface; and

(2) a second microelectronic element having a second body with a first surface, recesses in said body surface and metallic contact pads disposed in said recesses; so that said body surfaces confront one another and so that said bumps project into said recesses;

(b) bonding said bumps to said contact pads by a substantially ~~solid~~ solid-phase bonding process while urging said bodies toward one another so that at least some of said bumps, at least some of said contacts or both deform within said recesses.

18. (original) A method as claimed in claim 17 further comprising bonding said body surfaces to one another.

19. (original) A method as claimed in claim 18 wherein said step of bonding said body surfaces to one another is performed simultaneously with the step of bonding said bumps to said pads.

20. (original) A method as claimed in claim 18 wherein said step of bonding said body surfaces to one another includes activating a bonding material carried on at least one of said body surfaces.

21. (original) A method as claimed in claim 20 wherein said body surfaces are bonded to one another over substantially the entire body surfaces other than at said recesses and bumps.

22. (original) A method as claimed in claim 20 wherein said bumps, pads and recesses are disposed in one or more active regions of said body surfaces and said body surfaces are bonded to one another only in bonding regions outside of said active regions.

23. (original) A method as claimed in claim 22 wherein said bonding regions entirely surround each said active region.

24. (original) A method as claimed in claim 18 wherein at least one of said microelectronic elements is an active semiconductor element having one or more active electronic devices therein.

25. (original) A method as claimed in claim 18 wherein at least one of said microelectronic elements is a semiconductor chip.

26. (original) A method as claimed in claim 18 wherein at least one of said microelectronic elements is a semiconductor wafer.

27. (original) A method as claimed in claim 18 wherein said elements have substantially equal coefficients of thermal expansion.

28. (new) A method as claimed in claim 6 wherein, in each of said individual assemblies, at least some of the interconnect conductors connect active element contacts of the chip to one another to thereby provide routing of signals between portions of the chip.